## WHAT IS CLAIMED IS:

1	1. An apparatus, comprising:
2	a first voltage plane;
3	a signal layer on one side of the first voltage plane;
4	a second voltage plane on the other side of the first voltage plane; and
5	a floating trace on the signal layer, wherein the floating trace is electrically
6	connected to the second voltage plane.
1	2. The apparatus of claim 1, wherein the first voltage plane is a power plane and
2	the second voltage plane is a ground plane.
1	3. The apparatus of claim 1, wherein the first voltage plane is a ground plane and
2	the second voltage plane is a power plane.
1	4. The apparatus of claim 1, wherein the signal layer includes a plurality of
2	floating traces, each floating trace being (i) electrically connected to the second voltage
3	plane and (ii) not directly connected to other floating traces on the signal layer.
1	5. The apparatus of claim 1, wherein the floating trace and the second voltage
2	plane are electrically connected via a plated through hole.
1	6. The apparatus of claim 1, wherein the floating trace is a microstrip line.

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2	damping.
1 2	8. The apparatus of claim 6, wherein the microstrip line reduces resonance between the first voltage plane and the second voltage plane.
1 2	9. The apparatus of claim 1, wherein the first voltage plane, the signal layer, and the second voltage plane are separated by a dielectric material.
1	10. The apparatus of claim 1, wherein the apparatus is a printed circuit board.
1 2 3	11. The apparatus of claim 10, wherein the printed circuit board is associated with at least one of: (i) a flip chip ball grid array package model, and (ii) a pin grid array package model.
1 2	<ul><li>12. The apparatus of claim 1, further comprising:</li><li>a second signal layer.</li></ul>
1 2	<ul><li>13. The apparatus of claim 12, further comprising:</li><li>a second floating trace on the second signal layer.</li></ul>
1	14. A method, comprising:
3	providing a first voltage plane; providing a signal layer on one side of the first voltage plane;
4	providing a second voltage plane on the other side of the first voltage plane; and

7. The apparatus of claim 6, wherein the microstrip line provides impedance

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5	providing a floating trace on the signal layer, wherein the floating trace is
6	electrically connected to the second voltage plane.
1	15. The method of claim 14, further comprising:
2	positioning the floating trace in the signal layer to reduce cross-talk with a
3	neighboring signal line.
1	16. The method of claim 14 further comprising:
1	16. The method of claim 14, further comprising:
2	providing a second signal layer; and
3	providing a second floating trace on the second signal layer.
1	17. The method of claim 14, wherein providing the floating trace comprising:
2	providing a microstrip line on the signal layer.
1	18. A printed circuit board, comprising:
2	a signal layer including a plurality of microstrip lines that are not electrically
3	connected to each other on the signal layer;
4	a power plane under the signal layer and separated from the signal layer by a
5	dielectric material;
6	a ground plane under the power plane and separated from the power plane by the
7	dielectric material,
8	wherein each of the microstrip lines is (i) electrically connected to the ground
9	plane via a plated through hole passing through the dielectric material and the power
10	plane and (ii) not directly connected to other microstrip lines on the signal layer.

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1	19. The printed circuit board of claim 18, wherein the microstrip lines provide
2	impedance damping and reduce resonance between the power plane and the ground
3	plane.
1	20. A system, comprising:
2	a printed circuit board, including:
3	a first voltage plane,
4	a signal layer on one side of the first voltage plane,
5	a second voltage plane on the other side of the first voltage plane, and
6	a floating trace on the signal layer, wherein the floating trace is electrically
7	connected to the second voltage plane; and
8	a dynamic random access memory unit coupled to the printed circuit board.
1	21. The system of claim 20, further comprising:
2	a processor coupled to the printed circuit board, wherein the processor and
3	dynamic random access memory unit are to exchange information via signal lines on the
4	signal layer.